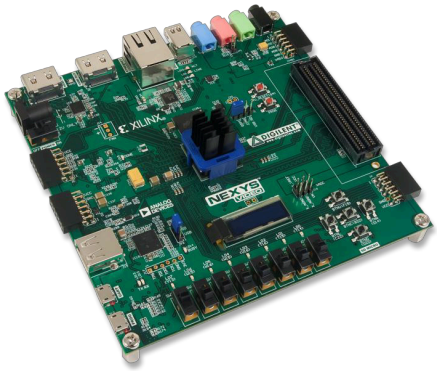
IronForge on Nexys Video

IronForge brings Linux, 720p60 HDMI, an onboard OLED splash, stereo analog playback and Gigabit Ethernet to the Nexys Video. HDMI and the OLED operate together on the physical board.

Platform	Board and runtime
FPGA / CPU	Artix-7 `xc7a200tsbg484-1` with 100 MHz MicroBlaze, MMU and caches
Memory	512 MiB physical DDR3. The default Linux policy exposes 256 MiB.
Common core	Linux 7.3.4, U-Boot 2026.10 and BusyBox 1.38.0
Network	IronKernel RTLNet MAC, RTL8211E-VL PHY and AMD AXI DMA in scatter-gather mode
Display and input	1280 × 720 at 60 Hz over HDMI, independent 128 × 32 SSD1306 OLED, UART and five board buttons
Audio and storage	ADAU1761 stereo analog codec, 32 MiB QSPI NOR, microSD over SPI and a Windows NFS option

Local display and control

U-Boot starts IronVideo scanout before Linux takes over the framebuffer. UARTLite provides the interactive console, with ordinary output mirrored to the HDMI text console. The OLED shows **IronKernel** during Linux startup. The framebuffer games use the HDMI display and accept keyboard or board-button input.



Digilent Nexys Video. Board photograph from the Digilent Nexys Video Reference Manual, page 3.

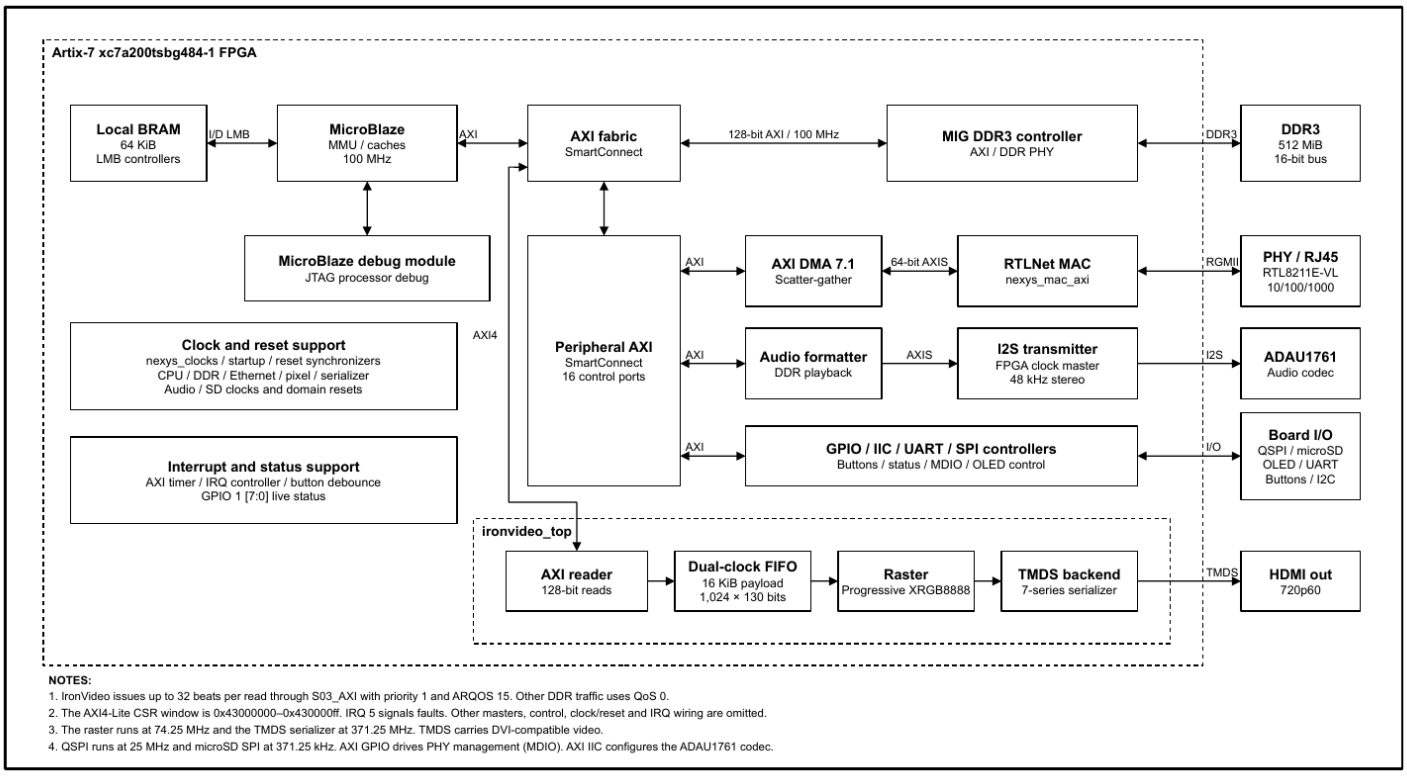
Boot and networking

The complete 32 MiB engineering image and the ZIP with programming instructions carry the same flash payload. Select Master SPI boot and open the USB serial console at 115200 baud. Games start from the shell. The operating system runs from RAM and mounts persistent storage at `/data`.

The programmed image passed flash verification and reached BusyBox after a power cycle with Ethernet disconnected. Linux registered both displays and the ADAU1761 sound card. With Ethernet connected, Windows retrieved live telemetry over the board's gigabit link.

FPGA and peripheral architecture

Figure 1. Nexys Video architecture with IronVideo DDR scanout and RTLNet scatter-gather Ethernet.



RTLNet and AXI DMA

AMD AXI DMA 7.1 has separate descriptor, RX and TX masters. Linux uses 128 RX and 64 TX descriptors, streaming DMA mappings and NAPI with a 40 µs coalescing delay. U-Boot uses two descriptors per ring.

Video and audio signal paths

IronVideo issues up to 32 beats on a 128-bit AXI4 read master at 100 MHz. The master interface and SmartConnect DDR port advertise 256-beat AXI4 capability. The reader enters SmartConnect through `S03_AXI` at priority 1 with `ARQOS=15`. A 16 KiB dual-clock RAM FIFO carries pixels and row and frame markers to the raster.

The programmable XRGB8888 raster uses CTA 720p60 with positive sync. Active, front porch, sync and back porch are 1280/110/40/220 pixels and 720/5/5/20 lines. A 74.25 MHz pixel clock and a 371.25 MHz serializer clock drive the 7-series DVI-compatible TMDS backend.

The OLED uses its own SPI controller. The ADAU1761 receives 48 kHz stereo audio at 24 bits in 32-bit I²S slots. The FPGA supplies a 12.288 MHz MCLK and a 3.072 MHz BCLK. The codec PLL derives 49.152 MHz. On Nexys, mpg123 requests a 0.8-second ALSA device buffer and attempts to raise its scheduling priority. At 48 kHz the kernel buffer holds 38,400 frames. Audio goes to the analog outputs on the board.

AMD catalog IP and canonical RTL

The native Vivado project configures the following board-level catalog cores.

AMD catalog type	Version	Instances or function
`microblaze`	11.0	`cpu`, 100 MHz with MMU and caches
`mig_7series`	4.2	`ddr`, 128-bit AXI to 512 MiB DDR3 over a physical 16-bit bus
`smartconnect`	1.0	`fabric` and `peripherals`, DDR and control interconnect
`axi_uartlite`	2.0	`uart`, 115200-baud serial console
`axi_timer`	2.0	`timer`, system timer interrupt
`axi_intc`	4.1	`intc`, interrupt aggregation
`axi_gpio`	2.0	`status`, `mdio`, `buttons` and `oledctrl`
`axi_iic`	2.1	`iic`, board I²C and codec configuration
`axi_dma`	7.1	`net_dma`, packet DMA and scatter-gather descriptors
`audio_formatter`	1.0	`formatter`, DDR playback stream
`i2s_transmitter`	1.0	`i2stx`, FPGA-master stereo I²S
`axi_quad_spi`	3.2	`flashspi`, `sdspi` and `oledspi`
`proc_sys_reset`	5.0	DDR and CPU-domain reset
`lmb_v10` / `lmb_bram_if_cntlr`	3.0 / 4.0	Local instruction and data buses and BRAM controllers
`blk_mem_gen` / `mdm`	8.4 / 3.2	64 KiB local BRAM and MicroBlaze debug
`xlconstant` / `xlslice` / `xlconcat`	1.1 / 1.0 / 2.1	Tie-offs, audio ID adaptation, interrupts and status

Authored and shared RTL

- **Ethernet.** RTLNet supplies the MAC. `nexys_mac_axi` bridges packet and control interfaces.
- **Video.** The board directly instantiates the shared `ironvideo_top` with its DDR reader, FIFO, raster, control registers and TMDS backend. The AXI4-Lite registers occupy `0x43000000` through `0x430000ff`. Scanout faults use interrupt 5.
- **Board support.** Nexys HDL provides clock generation, startup and reset sequencing, and button debounce.

The Linux `row_stats` attribute measures how many pixel clocks IronVideo takes to fetch one row. The driver uses the row size and elapsed cycles to report current and peak fetch bandwidth for this master. It also reports FIFO activity, underflows and read errors. Reading it clears the best and worst row latency measurements.

Console and terminal game

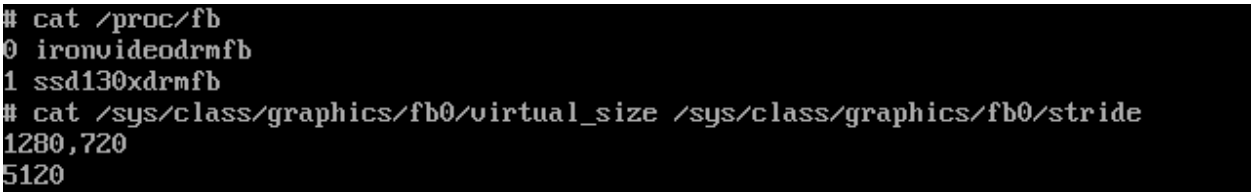


Figure 2. Excerpt from the framebuffer console showing both registered displays. Linux reports 1280 × 720 pixels on fb0 and a 5,120-byte row stride.

Serial and framebuffer console

U-Boot draws a blue XRGB8888 surface in the 4 MiB reservation at `0x90000000`. The Linux IronVideo DRM driver drains firmware scanout and takes over with a GEM DMA buffer from the 16 MiB CMA pool at `0x88000000`. HDMI registers as `ironvideodrmfb` on fb0. UARTLite handles input and mirrors ordinary output to VT1. The boot overlay requests unblank and draws the startup label on the separate SSD130x fb1.

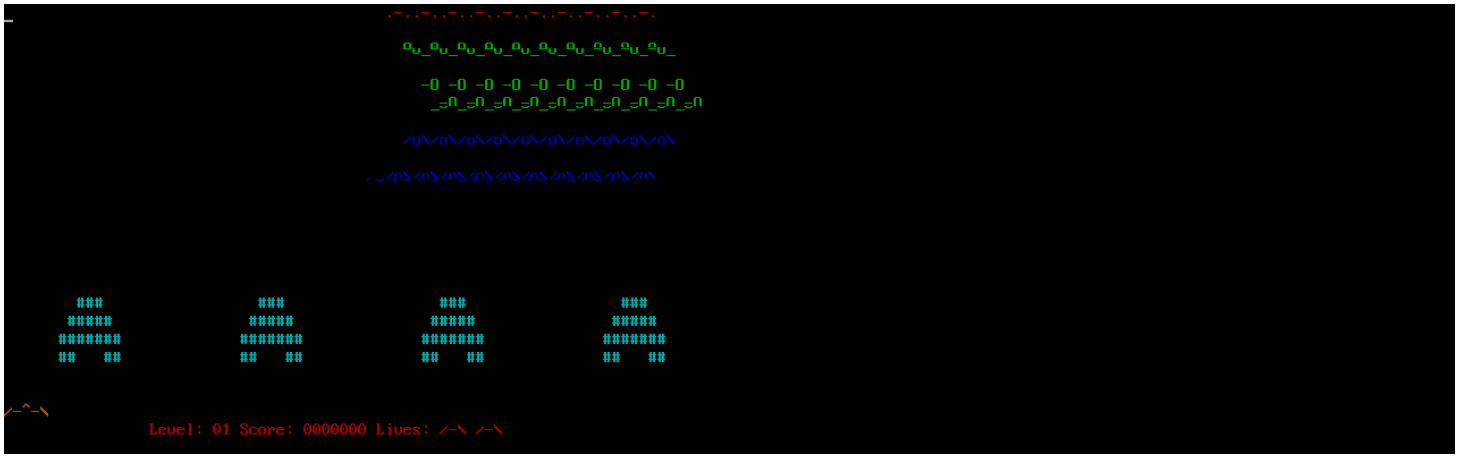


Figure 3. nInvaders text mirrored from the serial session to framebuffer memory. Run `ironforge-game` for the 80 × 30 terminal view. Press Space to start or fire, use the arrow keys to move, `p` to pause and `q` to exit.

Live dashboard and Ethernet

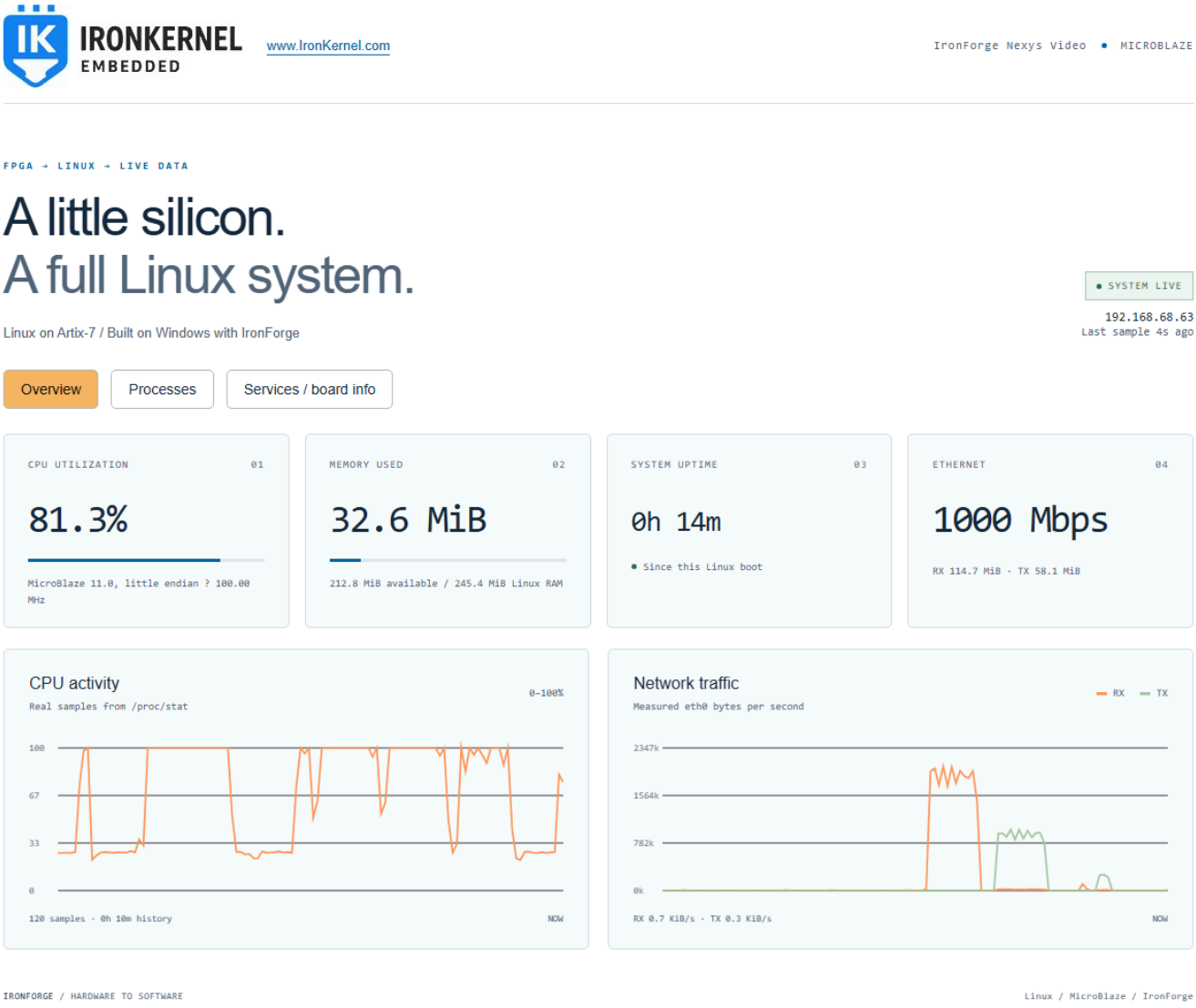


Figure 4. Live dashboard overview captured from the board. It shows CPU load, memory use, uptime, the negotiated Ethernet link rate and interface traffic counters.

Board telemetry

The RTLNet MAC and RTL8211E-VL PHY negotiate a 1 Gbps link. The dashboard reports the physical link rate and graphs measured interface traffic separately. Ethernet also carries DHCP, the web dashboard, MQTT telemetry and network boot traffic.

BusyBox HTTP serves the dashboard and invokes a native C telemetry helper. The visible tab polls every five seconds. A RAM-backed SQLite recorder retains up to 3,600 readings and can export them as CSV.

Processes and services

The Processes tab identifies tasks by user, PID, CPU use, resident memory and process state. The Services and Board Info tab summarizes HTTP and MQTT, broker connectivity, stored telemetry and software configuration.

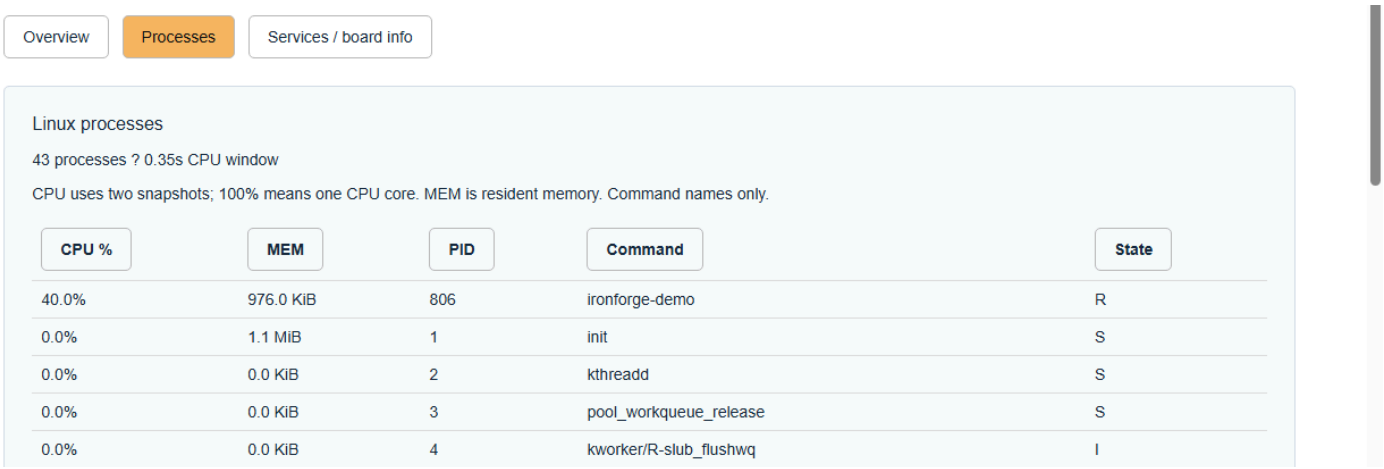


Figure 5. Processes tab captured after a warm return to SPI.

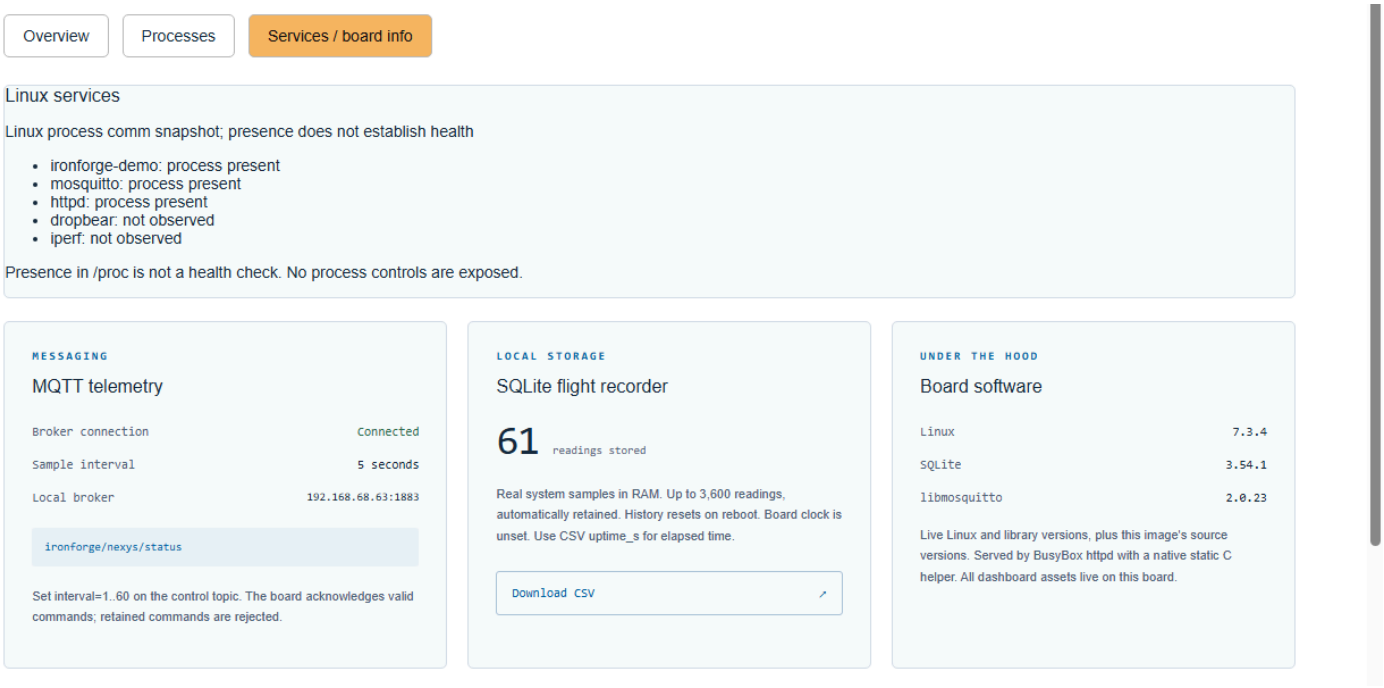


Figure 6. Services and Board Info captured after a warm return to SPI. Remote checks verified the HTTP response and a status message on `ironforge/nexys/status`.

Vector games and local input



Figure 7. Vector Defense framebuffer capture. Aim and launch interceptors to defend six cities.

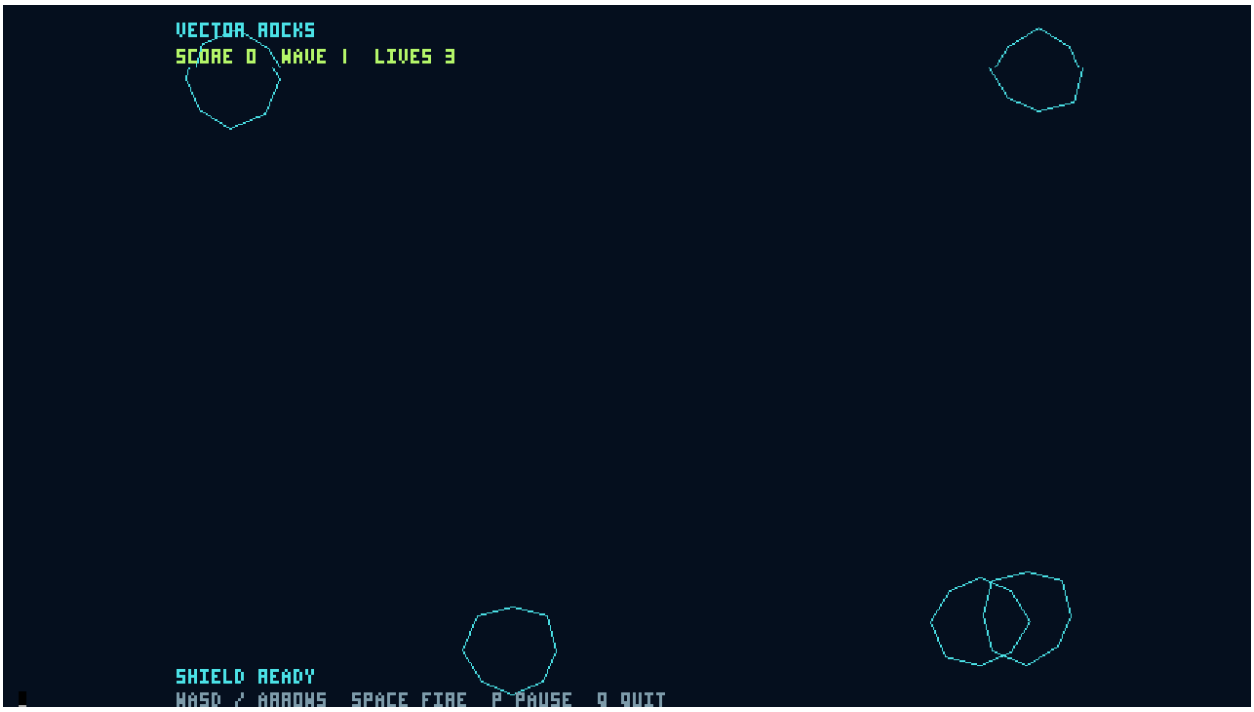


Figure 8. Vector Rocks framebuffer capture. Rotate, thrust and fire while avoiding rocks.

Both games center a 640 × 480 canvas at (320, 120) in 720p and paint black margins. On the board they switched to a graphics VT, preserved the black margins during injected serial output, and restored the console VT on exit. The captures illustrate the games. Physical button presses and display frame rate remain unverified.

Boot media and persistence

Two-file TFTP and writable NFS root

TFTP supplies `rootfs/boot/uImage` and `rootfs/boot/system.dtb`. U-Boot runs `bootm 82000000 - 84000000`, and Linux mounts the whole `rootfs/` share over NFSv3/TCP without an initramfs. Board qualification verified a board-written file on the Windows host and a persistent JFFS2 marker after returning to SPI.

Default offline flash layout

The loader in FPGA block RAM reads U-Boot from SPI flash into DDR. U-Boot checks the lengths and CRC32 values of the Linux uImage, external device tree and compressed initramfs as it reads them from raw flash. Linux mounts writable RAM as its root and persistent JFFS2 at `/data`. The `jffs2-root` variant keeps a full JFFS2 root with boot files.

Region	Start	Size
FPGA configuration and BRAM loader	`0x0000000`	10 MiB
U-Boot SREC	`0x0a00000`	5 MiB
Primary / redundant U-Boot environment	`0x0f00000` / `0x0f40000`	256 KiB each
Legacy Linux uImage	`0x0f80000`	4 MiB
External DTB	`0x1380000`	256 KiB
Compressed initramfs	`0x13c0000`	11.25 MiB
JFFS2 data	`0x1f00000`	1 MiB

Warm boot and removable storage

The installed flash image reached the shell in about 56 seconds from the first BRAM loader output on two warm boots, excluding FPGA configuration. Legacy LZ4 is the default initramfs format. The package also supports gzip for RAM boot and microSD rescue. Linux verified microSD automount and software eject.

Linux and RTLNet qualification

On November 20, the Digilent programming cable and USB-UART console on `COM3` passed board checks. The routed FPGA image met timing with +0.021 ns setup slack and +0.013 ns hold slack.

U-Boot selected the factory EEPROM MAC, saved it to SPI and recovered it on restart. The current two-file TFTP test booted Linux with a writable NFS root and no initramfs. Linux read matching EEPROM bytes, used the same MAC on `eth0`, obtained a DHCP address and negotiated 1 Gb/s full duplex. Ping passed in both directions. Six-second TCP tests measured 15.2 Mb/s from PC to Linux and 7.60 Mb/s from Linux to PC. Receive drops increased during the run, with zero receive or transmit errors reported. The earlier SPI image booted with a writable RAM root and used the locally administered fallback MAC.

After fresh JTAG programming, Linux 7.3.4 #28 reached BusyBox with a writable RAM root and the same factory MAC, `fc:0f:e7:00:e8:7a`.

Board verification and build workflow

Area	Verified behavior and scope
HDMI and OLED	A physical monitor displayed 720p60 and the onboard OLED displayed the startup splash. Live 720p60 samples showed frame progression with zero underflows, read errors or scanout faults.
FPGA and simulation	Native routing passed setup and hold. Independent serialized 720p60 and 1080p60 simulations checked timing and decoded frame pixels. 1080p60 is simulation coverage.
Board boot	The current display package booted from volatile JTAG RAM. The installed flash image separately passed warm SPI, writable NFS and return to SPI. Cold power-on remains open.
Analog audio	ALSA playback through the ADAU1761 reached the end of a 2:36 MP3 without underruns in JTAG RAM and quiet warm SPI trials. SPI playback tests with concurrent UART console activity recorded underruns. The codec routes playback to headphone and line-out outputs.
Memory and input	A 1 MiB U-Boot DDR scratch test passed. Full DDR coverage, physical button presses and physical microSD removal remain open.

Native Windows build

PowerShell and MSYS drive the AMD 2026.1 MicroBlaze and Vivado tools. The platform owns its board configuration and Vivado project under `platforms/nexys-video/`. The build shares pinned component inputs across boards and packages one generated `rootfs/`, which the Windows NFS server can export.

```
.\ironforge.cmd --platform nexys-video doctor
.\ironforge.cmd --platform nexys-video hardware --jobs 2
.\ironforge.cmd --platform nexys-video software all --jobs 2
.\ironforge.cmd --platform nexys-video package
```

BusyBox is static. Applications use the AMD hard-float sysroot and shared SQLite and ALSA libraries. Third-party packages retain their upstream terms. The common BRAM loader and vector games use MIT licenses.

Contact IronKernel

Integrate IronVideo HDMI scanout or RTLNet Ethernet into your AMD FPGA design with IronKernel. We also offer U-Boot and Linux board bring-up and custom drivers for display, audio and other peripherals.

To discuss integration, reference designs or custom development, send your target board and project goal.

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