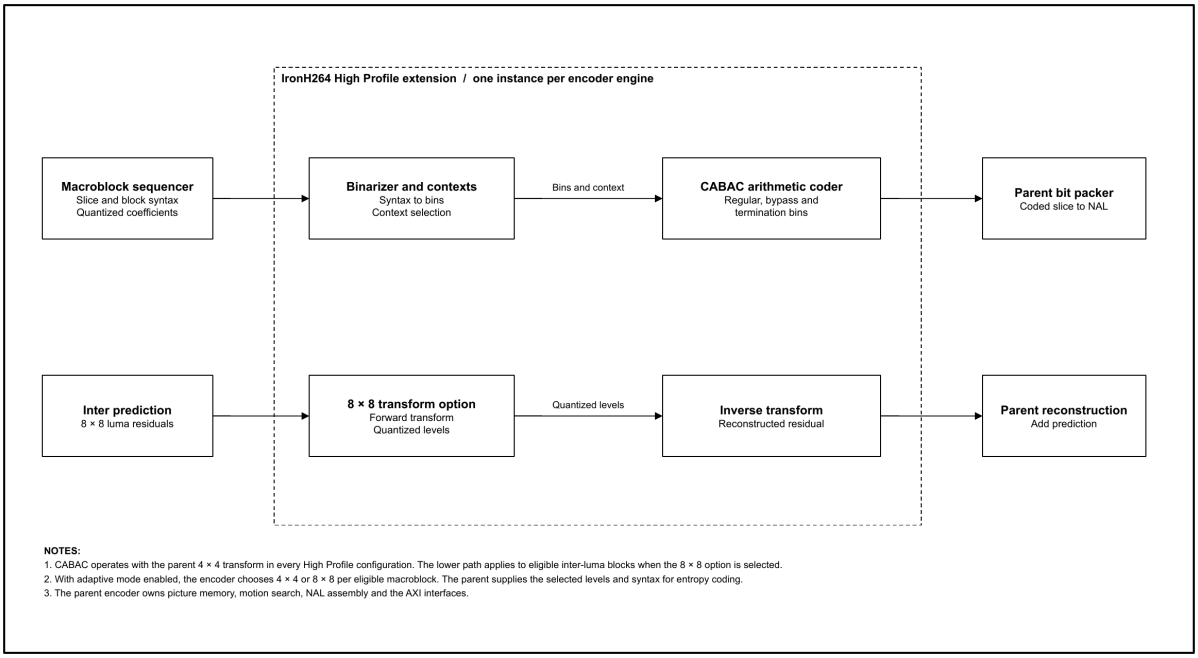
IRONKERNEL EMBEDDED

IronH264 High Profile Specification

IronH264 High Profile adds CABAC entropy coding and selectable inter-luma transforms to the IronH264 hardware encoder. It produces progressive, 8-bit H.264 High Profile video through the parent encoder's existing DDR and bitstream interfaces.

Markdown design guide for AI-assisted integration. Use the repository README with Claude or Codex to match encoder and netlist capabilities, configure the firmware, and verify profile transitions against an independent decoder.



Property	Contract
Coded stream	H.264 High Profile, profile_idc 100, 8-bit 4:2:0, progressive I and P slices
Tool selection	CABAC with 4 × 4 transforms, optional fixed inter 8 × 8, or adaptive inter 4 × 4 / 8 × 8
System interface	IronH264 AXI4-Lite registers, DDR source and reference buffers, compressed and index rings
Data path	Coefficient and residual interfaces inside each engine, followed by the shared bit packer
Delivery	Device-specific netlist with a declared tool set and full or timed operating mode

The Zybo Linux reference ships the Baseline encoder configuration. High Profile measurements in this document identify the reference platform or simulation explicitly.

Encoding tools and capabilities

Each enabled encoder engine contains one High Profile extension. The parent supplies prediction, picture memory, motion search, NAL packing and software-visible registers. The extension codes I and P slices with CABAC and, when selected, processes inter-luma residuals in 8 × 8 blocks.

Tool set	HP_STATUS capability nibble	Operations
CABAC	0x1	Context-adaptive binary arithmetic coding for intra and predicted slices. The parent uses its 4 × 4 transform path.
CABAC + inter 8 × 8	0x3	Adds four 8 × 8 luma residual blocks per inter macroblock and their reconstruction. Software may select fixed 8 × 8.
All tools	0x7	Adds per-macroblock selection between the inter 4 × 4 and 8 × 8 paths.

CABAC path. The macroblock sequencer supplies syntax elements to the binarizer. Context memory holds the adaptive states. The arithmetic coder handles regular, bypass and termination bins and emits commands to the shared bit packer. Slice initialization selects context state from slice type and QP.

Transform path. The parent supplies four inter-luma blocks in raster order, each as eight rows of eight signed samples. The extension transforms and quantizes the residual, retains coefficient levels for entropy coding, and inverse-transforms the quantized result for the parent reconstruction loop. Intra prediction and chroma retain their existing coding paths.

Adaptive selection. With adaptive mode enabled, the hardware estimates the cost of both transform sizes from the residual and quantization statistics. The chosen size is signalled per eligible inter macroblock. Fixed 8 × 8 and adaptive mode share the same picture parameter set. The counted population includes inter macroblocks with coded luma.

Host interface and picture boundaries

The extension shares the parent encoder address space. Software reads the tools actually present before choosing a mode. The following offsets are byte addresses relative to the encoder base.

Offset	Register	Interpretation
0x008	CAPS	Bit 20 identifies the High Profile interface in the parent build.
0x0C0	HP_CTRL	Bit 0 enables High Profile, bit 1 enables the inter 8 × 8 transform, bit 2 requests adaptive selection. Each feature is gated by the available tools. Adaptive requires bit 1.
0x0C4	HP_STATUS	Bits 0–3 indicate present, licensed, active and enable. Bit 4 is sticky PROFILE_CHG, cleared by writing one. Bits 5–6 report transform enable and adaptive choice. Bits 11:8 report tool capabilities. Bits 31:16 report remaining seconds.
0x0C8	HP_T8_COUNT	Last picture’s eligible inter macroblocks. Low 16 bits count 8 × 8 selections, high 16 bits count 4 × 4 selections across engines.
0x0D0 / 0D4	IRQ status / enable	Bit 3 reports a profile change, bit 4 loss of the timed operating mode. The parent’s picture-done and error events remain available.

1. Discover the interface and tool mask. Configure the parent source, reconstruction and rings. Choose CABAC alone, fixed inter 8 × 8 or adaptive operation.
2. At an accepted picture start the engine applies an enable or license transition. A change to the effective profile or picture-level transform signalling forces an IDR. A picture already in progress finishes under its original settings.
3. Read applied status and index flags. Prepend SPS/PPS matching the profile and transform mode to the IDR. Restart frame numbering at the transition so the receiver starts a fresh prediction sequence.
4. Use the picture and transform counters together. A zero transform count can mean the picture had no eligible inter-luma blocks.

System integration and operating modes

The extension runs on the encoder clock. A macroblock command starts while the module is idle. Coefficient reads use the parent’s synchronous coefficient store. Encoded commands use valid/ready flow control through to the shared bit packer. Because the parent owns all AXI memory transactions, input layout, DMA addressability and ring ownership follow the IronH264 integration.

Configuration	Observable behavior
Full netlist	The licensed indication stays asserted. Remaining time reads 0xFFFF.
Timed evaluation	The reference evaluation interval is 30 minutes from FPGA configuration. The counter uses the configured encoder clock. Software reads remaining seconds through HP_STATUS.
Timed interval ends	The current picture completes. At the next accepted start the engine forces an IDR and continues with Constrained Baseline CAVLC. Software supplies matching parameter sets.
Timing and device selection	The delivered netlist must match the FPGA part and tool configuration. Verify the complete design’s routed timing at the intended encoder clock.
Recorded Nexys Video example	The Artix-7 XC7A200T reference demo uses a 90 MHz, 30-minute CABAC-only netlist. Its recorded tool flags disable inter 8 × 8 and adaptive selection.
Zybo Z7-20	The High Profile option is reserved for private benchmarking. The public Zybo streaming measurements apply to the Baseline encoder.

A receiver should be able to join on each IDR and decode through a profile transition. Compare the reported output profile, the parameter sets in the stream and the IDR flag in the picture index.

Compression and verification

These figures are recorded RTL simulation results. Each row sums the two P pictures in an IPP sequence, at QP 28, using one engine and one slice. The inputs and QP are identical across the three columns. Smaller values indicate fewer coded bits for these pictures.

Sequence	Baseline CAVLC bits	High CABAC 4 × 4 bits	High CABAC fixed 8 × 8 bits
720p scrolling bars	16,728	8,528	8,368
720p pan	9,464	7,320	7,800
1080p moving objects	2,640	3,016	3,016

The pan used fewer bits with CABAC and the 4 × 4 transform than with fixed 8 × 8. The short 1080p objects sequence used fewer bits with Baseline. Evaluate representative scenes at the required quality and frame deadline. Report coded bits, reconstructed quality and cycles per picture together.

Independent verification compares emitted slice bytes with a reference model and decoded pictures with the encoder reconstruction. The recorded tool-set regression includes QCIF, 720p and 1080p cases, one- and two-engine configurations, and deblocking enabled and disabled. JM, OpenH264 and FFmpeg supply independent decode checks. License-transition tests check the forced IDR and continued decoding across the change.

Contact IronKernel

For High Profile evaluation, include the FPGA part, encoder clock, target bitrate, quality metric and a representative video sequence. These inputs guide selection of the CABAC and transform options.

IronKernel provides FPGA design and design review, board bring-up, bare-metal firmware, embedded Linux drivers and application development. For integration support, a reference design or a custom development proposal, send your target board and project goal.

IronKernel.com · support@ironkernel.com